PATENT APPLICATION
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PORTABLE COMPUTER HAVING DUAL CLOCK MODE

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The Field of the Invention

The present invention generally relates to portable computers and more
5   particularly, to a portable computer having a dual clock mode system and
method for optimizing system performance and extending battery life.

Background of the Invention

Mobile computing devices or portable computers, such as laptop
10   computers, have become increasingly popular. Mobile computing devices are
battery powered in order to enhance their portability. A battery powered laptop
computer operates for an extended period of time under battery power before the
battery is either recharged or replaced. Alternatively, the mobile computing
device may be powered from an external power source, such as an alternating
15   current (AC) power source. As processor speeds and memory capacities of
mobile computing devices have increased, so has their power consumption. At
the same time, mobile computing devices have become increasingly smaller in
size and weight.

It is important to reduce power consumption within an electronic circuit
20   of the laptop computer, in order to extend the period of time during which the
electronic circuit operates before recharging or replacing the battery. Known
techniques disable power or disable clock signals (e.g., in a "sleep" or idle
mode) to the electronic circuit in response to a specific time elapsing without
sensing a particular type of activity. As such, it is desirable to limit the battery
25   size within the mobile computing device.

Processor and memory bus clock speed corresponds directly to the
amount of power required by the mobile computing device. Specifically, a faster
clock speed results in increased power consumption, and a slower clock speed
results in decreased power consumption. As such, most laptop computers are
30   built with a clock speed which is much slower than similarly sized desktop
computers, in order to reduce the power consumption and extend the amount of

time that the laptop computer can be powered by a battery. It is desirable to have a mobile computing device which operates at a slower clock speed while battery powered, but is capable of operating at a higher clock speed when connected to an external (e.g., AC) power source.

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Summary of the Invention

The present invention provides a portable computer. In one aspect, the portable computer has a first power mode and a second power mode. The portable computer includes a memory bus and a control system coupled to the

10   memory bus. The control system is configured to operate the memory bus at a first speed in the first power mode and a second speed different than the first speed in the second power mode.

Brief Description of the Drawings

15   Figure 1 is a perspective view illustrating one exemplary embodiment of a portable computer according to the present invention.

Figure 2 is a block diagram illustrating one exemplary embodiment of the portable computer of Figure 1.

Figure 3 is a block diagram illustrating one exemplary embodiment of a

20   portion of a portable computer according to the present invention.

Figure 4 is a diagram illustrating one exemplary embodiment of a graphical user interface used in a portable computer according to the present invention.

Figure 5 is a flow chart illustrating one exemplary embodiment of a

25   method of managing power in a portable computer according to the present invention.

Description of the Preferred Embodiments

In the following detailed description of the preferred embodiments,

30   reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may

be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

5   Figure 1 is a perspective view illustrating one exemplary embodiment of a portable computer 20 according to the present invention. Portable computer 20 has a first power mode (e.g., a battery power mode) 22 and a second power mode (e.g., an external power mode) 24. In the first power mode 22, the portable computer 20 memory bus is operated at a first speed (e.g., a slow clock

10 speed), and in the second power mode 24, the portable computer 20 memory bus is operated at a second speed different from the first speed (e.g., a fast clock speed).

By operating the memory bus at a relatively slow clock speed in the first power mode 22, power consumption by the portable computer 20 is reduced.

15 This results in extending the amount of time that the mobile portable computer 20 can be operated in the first power mode 22. In the second power mode 24 the mobile computing device's memory bus is operated at a faster speed, resulting in improved performance of the portable computer 20. The increased operating speed results in more power consumption by the portable computer 20. Since in

20 the second power mode 24 the portable computer 20 is powered via an external power source, a user is no longer concerned about the increased power consumption due to increasing the speed of the memory bus. The portable computer 20 may include other "power saving" components, such as changing the processor clock speed to components within the control system (e.g.,

25 entering a sleep mode) in addition to changing memory bus speed.

In one exemplary embodiment illustrated, the portable computer 20 is a laptop computer or a notebook computer. The term "portable computer" or "mobile computing device" as used herein also extends to other known mobile computing devices such as personal digital assistants (PDAs), or other devices

30 having a first battery power mode and a second external power mode.

Figure 2 is a block diagram illustrating one exemplary embodiment of the portable computer 20 of Figure 1. Portable computer 20 includes control system 30, memory 32, input devices 34, data storage devices 36, display 38, peripheral devices 40, modem 42, wireless port 44 and input/output port 46. Control

5   system 30 provides for operation of the portable computer 20. Control system 30 includes a microprocessor having a set of internal instructions stored in memory and provides for the transfer of data and instructions between control system 30 and memory 32. In one aspect, memory 32 includes random access memory (RAM) 60 and read only memory (ROM) 62. In one aspect, control

10   system 30 provides for the reading of operational instructions or code from ROM 62, and the reading and writing of data at RAM 60. In one embodiment, RAM 60 is dynamic random access memory (DRAM). Control system 30 can receive instructions or data from input devices 34, such as a keyboard 50, a mouse 52 or other input device 54. Control system 30 can receive and store data

15   from various types of data storage devices 36, such as hard disk drive 70, floppy disk drive 72, or CD/DVD drive 74. Control system 30 can display data via display 38 as known in the art. Control device 30 can send data to peripheral devices 40 (e.g., a printer), or output and receive data via modem 42, wireless port 44, or input/output port 46.

20   Portable computer 20 is operable in a first power mode or a second power mode. In the exemplary embodiment shown, portable computer 20 is operable in the first power mode 22 via battery 70. Portable computer 20 is operable in a second power mode 24 via connection to an external power source 72. In one aspect, the external power source is an alternating current (AC)

25   power source such as a 120 volt AC power source.

Controller system 30 includes a power manager 80, a power mode detector 82, and a clock generator 84. Power mode detector 82 and clock generator 84 are in communication with power manager 80. In one aspect, a first memory bus 86 is provided between controller system 30 and RAM 60 and

30   a second memory bus 88 is provided between control system 30 and ROM 62. A first clock bus 90 is provided between control system 30 and RAM 60, and a

second clock bus 92 is provided between control system 30 and ROM 62. Clock bus 90 determines the speed in which data is transferred between control system 30 and RAM 60 via first memory bus 86, and clock bus 92 determines the speed at which data is transferred between control system 30 and ROM 62 via second

5   memory bus 88.

Power manager 80 operates to "manage" the power use of portable computer 20. In particular, power manger 80 operates to reduce power consumption by portable computer 20 when operating in a first power mode in 22 via battery 70. Power manager 80 operates to maximize system performance

10   of portable computer 20 when portable computer 20 is in a second power mode   .
24 and connected to an external power source at 72. Power manager 80 can be implemented via software, hardware, or a combination of software and hardware.

In one aspect, power mode detector 82 determines whether the portable

15   computer 20 is operating in a first power mode 22 or a second power mode 24, and provides a corresponding output signal 100 to power manager 80. In response to the output signal 100 received from power mode detector 82, power manager 80 provides a corresponding output signal 102 to clock generator 84 determining the desired speed at which clock generator 84 is to output clock

20   signals on clock bus 90 and clock bus 92. In one exemplary embodiment, power mode detector 82 determines that portable computer 20 is operating in a first or battery power mode 22, and provides a corresponding output signal 100 to power manager 80. In response, power manager 80 provides an output signal 102 to clock generator 84, indicating that portable computer 20 is to provide an output

25   clock signal to clock bus 90 and clock bus 92. The output clock signal operates to transfer data via memory bus 86 and memory bus 88 at a first or slow speed, since the portable computer 20 is operating from battery 70 and as such it is desirable to reduce power consumption by the portable computer 20.

In another aspect, power mode detector 82 determines that the portable

30   computer 20 is being powered in a second power mode 24 via an external power source 72. Power mode detector 82 provides a corresponding output signal 100

to power manager 80. In response, power manager 80 provides a corresponding output signal 102 to clock generator 84. Clock generator 84 responds by providing a fast clock signal output to clock bus 90 and clock bus 92 for determining the speed of data transferred via memory bus 86 and memory bus

5   88. In one aspect, the clock signal provided by clock generator 84 in the first power mode 22 is the same as the clock signal provided by clock generator 84 in the second power mode 24. In another aspect, the clock signal provided in the second power mode 24 is different than the clock signal provided in the first power mode 22. In one aspect, the clock signal in the second power mode 24 is

10   faster than the clock signal in the first power mode 22. In one exemplary embodiment, the clock signal provided in the second power mode 24 is double the speed of the clock signal provided in the first power mode 22 (e.g., a first power mode clock speed of 66 megahertz, and a second power mode clock speed of 133 megahertz).

15   Figure 3 is a block diagram illustrating a portion of mobile computing device 20 including control system 30 and memory 32. In one aspect, control system 30 includes a processor 110 and a chipset 112. Chipset 112 provides for controlling data transfers between the processor 110 and other devices internal and external to portable computer 20, such as performing the functions of

20   controlling temporary or cache memory, performing direct memory access (DMA), handling interrupt, transferring data via the I/O port, etc. In one aspect, chipset 112 includes one or more application-specific integration circuits (ASICs). One suitable chipset is commercially available from Intel Corporation.

          In one exemplary embodiment, chipset 112 includes power manager 80

25   and power mode detector 82. Chipset 112 is in communication with clock generator 84. Clock generator 84 may be located internal to chipset 112, or external to chipset 112 either inside of control system 30 or external to control system 30. In one aspect, memory 32 includes RAM 60 configured as a "memory bank" of RAM chips, indicated as memory M1 120, memory M2 122,

30   memory M3 124, memory MN 126. Each memory chip is in communication with control system 30 via memory bus 86. The memory bus speed or the speed

at which data is transferred via memory bus 86 is determined by clock bus 90. As previously described herein, power mode detector 82 determines whether portable computer 20 is operating in a first power mode 22 or a second power mode 24. In response, power manager 88 determines the clock speed provided

5   by clock generator 84 to clock bus 90.

Portable computer 20 may further include a performance level input 130, which may be input or defined via an input device 34. Performance level input 130 provides a method for defining the memory bus speed for first power mode 122 and second power mode 24. In one aspect, the performance level input 130

10   is input to control system 30 via a graphical user interface (e.g., a window-based user interface).

In one embodiment, RAM 60 is DRAM, having an access speed corresponding to the memory bus speed. Exemplary embodiments of DRAM technology suitable for use with the present invention includes conventional

15   DRAM, page mode, FPM, EDO, BEDO, Synchronous DRAM (SDRAM), DDR SDRAM, DRDRAM, SLDRAM. Other suitable memory technologies will become apparent to one skilled in the art after reading the present application.

Figure 4 is a diagram illustrating one exemplary embodiment of a graphical user interface for use as a performance level input 130 according to the

20   present invention. The graphical user interface 150 is used as part of power manager 80 for defining the memory bus speed for a first power mode 22 and a second power mode 24. In one aspect, graphical user interface 150 includes a battery power mode field 152, an external power mode field 154, and a power mode over-ride setting for battery and external power mode 156. In the battery

25   power mode 152, a user may select a slow memory bus speed 160 or a fast memory bus speed 162. The slow memory bus speed 160 and fast memory bus speed 162 can be predefined based on the components of the specific portable computer 20, such as the speed of RAM 60 and control system 30. In one exemplary embodiment, the slow memory bus speed 160 is 66 megahertz and

30   the fast memory bus speed 162 is 133 megahertz. Alternatively, the battery power mode 152 may select a user defined memory bus speed 164. If a user

defined memory bus speed 164 is selected, an active field 166 is provided for allowing the user to input the desired memory bus speed in the battery power mode 152.

Similarly, in the external power mode 154 a user may select a slow

5   memory bus speed 170, a fast memory bus speed 172 or a user defined memory bus speed 174. Again, if the user defined memory bus speed 174 is selected, an active input field 176 is provided for allowing the user to input a desired memory bus speed.

Situations may exist when it is desirable for a user to over-ride the

10   default or defined settings for the battery power mode 152 and external power mode 154. As such, battery power mode over-ride setting for battery in external power mode 154 is provided to predefine such a situation. Again, a user may select a slow memory bus speed 180, a fast memory bus speed 182, or a user defined memory bus speed 184. If the user defined memory bus speed 184 is

15   selected, a user is provided with an active input field for inputting a desired memory bus speed, indicated at 186. In one aspect, the power mode over-ride setting provides the memory bus speed for both the battery power mode 152 and the external power mode 154, and as such, the memory bus speed for the battery power mode 152 and the external power mode 154 will be the same.

20   Figure 5 is a flow chart illustrating one exemplary embodiment of a method of managing power in a mobile computer system, according to the present invention.

At 202, it is determined whether the portable computer is operating in a first power mode or a second power mode. At 204, the memory bus is operated

25   at a first bus speed when the mobile computing device is in the first power mode (e.g., a battery power mode). At 206, the memory bus is operated at a second bus speed different from the first bus speed when the mobile computing device is in the second power mode (e.g., an external AC power source).

Although specific embodiments have been illustrated and described

30   herein for purposes of description of the preferred embodiment, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate

and/or equivalent implementations calculated to achieve the same purposes may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. Those with skill in the chemical, mechanical, electro-mechanical, electrical, and computer arts will

5   readily appreciate that the present invention may be implemented in a very wide variety of embodiments. This application is intended to cover any adaptations or variations of the preferred embodiments discussed herein. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

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